REMARKS

Claims 1-7, 9-23, and 27-34 are pending. Claims 1, 13, 18, and 27 are in independent form.

No new claim amendments are proposed at this time. The amendments to claims 1, 13, 18, and 27 proposed in the response filed August 8, 2005 are not entered for purposes of appeal but are nevertheless denoted in the Listing of Claims as "previously presented."

CLAIM 1

In the Advisory Action mailed September 13, 2005, it was indicated that the rejection of claim 1 under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 6,094,729 to Mann (hereinafter "Mann"), U.S. Patent No. 5,553,010 to Tanihara et al. (hereinafter "Tanihara"), and U.S. Patent Publication No. 2003/0115424 to Bachand et al. (hereinafter "Bachand") would be upheld.

In indicating that the rejection would be upheld, the Advisory Action made two contentions as to why the rejection was proper.

The first of these contentions is that one of ordinary skill could add trace comparison techniques to Mann's trace compression based on disruptions to the program flow "since some

of Mann's traces do involve address values" and "a trace comparison compression method *could still be used for instances where further compression is desired...*" (emphasis added).

However, the mere fact that it is not impossible to practice the claimed subject matter in Mann's system is insufficient to establish a *prima facie* case of obviousness in reliance upon Mann. In particular, there has been no showing of *some suggestion or motivation to combine the references to achieve the claimed subject matter*. Such a suggestion or motivation must be *founded in the prior art* and not drawn from Applicant's own disclosure.

In this case, Mann is the *only cited reference* that involves trace compression. Mann describes that trace compression is to be achieved on the *basis of disruptions to the program flow*, not comparisons of address pairs. Further, Mann's trace compression technique discards at least some of the addresses, that are compared in the claimed subject matter.

These facts speak to the motivations of one of ordinary skill, who would have to overcome both Mann's express teachings as to how trace compression is to be achieved and Mann's potential discarding of information that is relied upon in the claimed trace compression. The mere fact that it is not

impossible to practice the claimed subject matter in Mann's system does not imply that one of ordinary skill would find some affirmative suggestion or motivation to practice the claimed subject matter.

Indeed, no basis for believing that one of ordinary skill would be so motivated has been established. Instead, the rejection asserts that one of ordinary skill would spontaneously disregard Mann's teaching that trace compression is to be based on disruptions to the program flow and instead apply Bachand's cache coherency checking and Tanihara's data shifter circuit to somehow arrive at the claimed trace compression. Absent a suggestion or motivation founded in the prior art, such a bald assertion is insufficient to carry the Office's burden of proof. Accordingly, a *prima facie* case of obviousness has not been established and the rejection of claim 1, and the claims dependent therefrom, cannot be sustained.

The second of the contentions indicating that the rejection of claim 1 would be upheld is that Bachand's single observation detection logic 246 somehow constitutes both a first comparator to compare a new branch target address corresponding to a loop in the first holding register to a stored branch target address in the first end register and a second comparator to compare a

new branch source address corresponding to the loop in the second holding register to a stored branch source address in a first adjacent register. The alleged basis of this equivalence is the performance of successive comparisons by observation detection logic 246.

To begin with, applicant submits that the performance of successive comparisons by a single comparator does not transform the single comparator into multiple comparators. As recited in claim 1, the first comparator is to compare a new branch target address corresponding to a loop in the first holding register to a stored branch target address in the first end register, whereas the second comparator to compare a new branch source address corresponding to the loop in the second holding register to a stored branch source address in a first adjacent register. The comparators thus compare different data to achieve different comparisons results and are not the same single comparator.

Further, the Advisory action contends that external transaction queue 240 is a first end register. The first end register of claim 1 is to "input and output addresses of fetched instructions." By contrast, external transaction queue 240 is populated by queue entries (i.e., "ETQ entries") for each pending bus transactions. See Bachand, para. [0036]. Applicant

submits that such pending bus transactions are not fetched instruction. Rather, such pending bus transactions are pending.

Therefore, even if Mann, Tanihara, and Bachand were combined, then one of ordinary skill would still not arrive at the claimed subject matter. In particular, none of Mann, Tanihara, and Bachand describe or suggest a first comparator to compare a new branch target address corresponding to a loop in the first holding register to a stored branch target address in the first end register and a second comparator to compare a new branch source address corresponding to the loop in the second holding register to a stored branch source address in a first adjacent register.

Since claim elements and/or limitations are neither described nor suggested by Mann, Tanihara, and Bachand, a *prima facie* case of obviousness has not been established. Therefore the rejection of claim 1, and the claims dependent therefrom, cannot be sustained.

CLAIM 13

In the Advisory Action mailed September 13, 2005, it was indicated that the rejection of claim 13 under 35 U.S.C. § 103(a) as obvious over Mann and Tanihara would be upheld.

In indicating that the rejection would be upheld, the Advisory Action contends that FIG. 2 of Mann discloses "parallel processing attributes" and that such attributes somehow constitute a pipelined processor.

FIG. 2 of Mann shows a processor device 102 that includes a processor core 104 and may incorporate "additional circuitry… for performing application specific functions." *See Mann*, col. 4, line 15-26. Even if this "additional circuitry" were taken to be additional processors, there is no reason to believe that the additional processors would be pipelined processors. Further, there is no reason to believe that Mann's trace compression techniques would be applied to the additional processors, especially when Mann describes that it is to be applied to processor core 104.

Thus, even if Mann were taken to disclose "parallel processing attributes," such attributes neither describe or suggest a pipelined processor at all, much less the pipelined processor recited in claim 13.

Since claim elements and/or limitations are neither described nor suggested by Mann and Tanihara, a *prima facie* case of obviousness has not been established. Therefore the

rejection of claim 13, and the claims dependent therefrom, cannot be sustained.

Applicant asks that all claims be allowed. Please apply the Petition for Extension of Time fee to Deposit Account No. 06-1050. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

BY
JOHN F. CONROY
REG. NO. 45,485

Date: September 30, 2005

Scott C. Harris
Reg. No. 32,030
Attorney for Intel Corporation

Fish & Richardson P.C.
PTO Customer No. **20985**
12390 El Camino Real
San Diego, California 92130
(858) 678-5070 telephone
(858) 678-5099 facsimile

10555603.doc